“SPICE Compatible Models for Circuit Simulation of ESD Events”

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MOTIVATION

Key Drivers: the 3 “S”

- **Simulation**: Predicting robustness of a particular design to ESD prior to manufacture.

- **Synergy**: Synthesize the physical concepts that describes the ESD event into a self-contained solution.

- **Simplicity**: Automate and integrate simulation flow in a standard circuit simulation environment.
OUTLINE

1) What is ESD?
2) Modeling Objectives & Approach
3) Model Development
4) Circuit Simulation Examples
5) Concluding Remarks
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What is ESD?

Definition: Electro-Static Discharge

Relevance: - Damages IC
            - Key “product quality” metric

Customer Return Pareto:
What is ESD?

Designing for ESD Robustness: Common Practice

Design cycle:
What is ESD?

Designing for ESD Robustness: The benefit of Simulation

Design cycle:
OUTLINE

1) What is ESD?
2) Modeling Objectives & Approach
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5) Concluding Remarks
Modeling Objectives & Approach

A. Verification
   - Pass or Fail Robustness test
   - Interaction with Core (or Protected) Circuitry

B. Optimization
   - Redundant or insufficient protection?

C. Design Cycle Reduction
   - First pass success

D. Simplicity
   - Adopted by end-user
Modeling Objectives & Approach

Quantify Charge dissipation and Failure
Modeling Objectives & Approach

Device Model Development Characteristics: \textit{ASIIC}

- Accurate
- Simple
- Incremental
  - Leverage standard device models.
- Integrated
  - Compatible with circuit design environment.
- Comprehensive
  - Protection as well as protected devices modeled.
Modeling Objectives & Approach

ESD Characteristics

A. Electrical:
   - Large currents & large voltages
   - Short duration: 1-200 ns.

B. Physical Failure:
   - Junction damage
   - Dielectric/Gate-oxide damage
Modeling Objectives & Approach
ESD Characteristics

C. Limited applied stimulus:

- Two common models: HBM & CDM
Modeling Objectives & Approach
What to model?

- Focus on region beyond normal operation.
- Determine failure point.

![Diagram showing voltage and current relationships with device failure and normal operation zones.](image-url)
Modeling Objectives & Approach

What to model?

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Modeling Objectives & Approach
Modeling Objectives & Approach

Measuring DUT Transient Characteristics

Characteristics obtained using a TLP (transmission line pulse) measurement technique.
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Model Development
What to model?

SiGe Complementary Bipolar Process
Proprietary high performance fully dielectrically isolated complementary bipolar process with SiGe NPN.
Model Development

Incentive for Device Model Development
Model Development

What Devices to Model?

A. Core Devices:
   - Bipolar transistors: PNP & NPN
   - Diodes
   - Passive Devices

B. Protection Devices:
   - ESD Diodes
Model Development

Physical Mechanisms to Model

- Junction Breakdown
- Avalanche Current
- Velocity Saturation
- Kirk Effect
- Resistivity Modulation
- Failure
Non-Physical Diode-Switch Model

- **Verilog-A Implementation:**
  - Variable "turn-on" Voltage: \( V_{on} \)
  - Variable series Resistance: \( R \)

![Diagram of a diode switch with variables \( V_{on} \) and \( R \)](image-url)

![Graph showing current and voltage with \( V_{on} \) and \( R \)](graph-url)
Model Development

ESD Diode Model

Standard operation

Operation during ESD event
Model Development

ESD Diode Model

- Sub-circuit consisting of Ideal and Standard diodes.
Model Development

Bipolar Breakdown Models

- $BV_{EBO}$: Emitter-Base junction breakdown with Collector floating.
- $BV_{CBO}$: Collector-Base junction breakdown with Emitter floating.
- $BV_{CEO}$: Collector-Emitter breakdown with Base floating.
Model Development

Leverage and Integrate with Standard SPICE Model

- Start with MEXTRAM model
- Add necessary elements to model high-current/voltage transient.
NPN Emitter-Base Breakdown Model

- NPN $BV_{EBO}$ is modeled using:
  - Ideal diode: $D1$
  - Series resistance: $R1$
  - DC source: $VEBO = BV_{EBO}$
- Diode turns on at $VEBO$

NPN $AE = 0.35 \times 5.2 \mu m$

Device Failure ($VM, IM$)

**Diagram:**
- Circuits and graphs showing current vs. voltage characteristics for the model.
Model Development

PNP Emitter-Base Breakdown

TLP I-V Characteristics

![Graph showing TLP I-V Characteristics](image)

- **Device Failure** ($V_M, I_M$)
- $BVE_{B0}$

PNP $A_E = 4 \times 1 \times 10 \mu m$

- **POLYSILICON**
- **EXT-BASE**
- **PRIMARY**
- **SECONDARY**
- **PSUB**
- **P-BL**
- **TRENCH**
- **OXIDE**

![Cross-section diagram of a device](image)
Model Development

PNP Emitter-Base Breakdown Model

- A parallel breakdown is observed at $V > BV_{EBO}$
- This breakdown is modeled using:
  - Ideal diode: $D_2$
  - Series resistance: $R_2$
  - DC source: $V_{EBO1} = BV_{EBO1}$

![Diagram of PNP Emitter-Base Breakdown Model]

- Device Failure ($V_M, I_M$)
- Primary ($R_1$)
- Parallel ($R_2$)
- $PV_{EBO} = 4 \times 1 \times 10 \mu m$
Model Development

NPN Collector-Base Breakdown Model

- $BV_{CBO}$ is modeled using:
  - Ideal diode: $D2$
  - Series resistance: $R2$
  - DC source: $V_{CBO} = BV_{CBO}$

- Diode turns at $V_{CBO}$
Model Development

PNP Collector-Base Breakdown

*Pulsed I-V Characteristics*

![Graph showing pulsed I-V characteristics with device failure marked by a dotted line.](image)

- **CURRENT (mA)**
- **VOLTAGE (V)**

**PNP $A_E=1 \times 10^{-12}$m**

**Device Failure** ($V_M, I_M$)

**$BV_{CBO}$**

**Layers and Regions**:
- **POLYSILICON**
- **EXT-BASE**
- **SECONDARY**
- **PRIMARY**
- **TRENCH**
- **OXIDE**
- **PSUB**
- **P-BL**

**Points**:
- **E**
- **B**
- **C**
Model Development

PNP Collector-Base Breakdown Model

- A Parallel breakdown path is observed due to the reach-through between extrinsic-base/collector.
- Current flows laterally instead of vertically.

![PNP Collector-Base Breakdown Model Diagram]

Device Failure ($V_M, I_M$)

- PARALLEL (R2)
- PRIMARY (R1)
- $BV_{CB0}$

Graph showing CURRENT (mA) vs VOLTAGE (V)
Model Development

Collector-Emitter Breakdown

- Impact ionization in the base collector depletion region.
- Electron-hole pairs swept into the base and collector respectively.
- Results in forward-biasing the base-emitter base junction.
- Current flow from emitter to collector sustains the avalanching in the depletion region.
Model Development

Collector-Emitter Breakdown Model

- The collector-emitter breakdown characterized by several physical mechanisms.
- Primary breakdown is due to avalanche.
- Carrier velocity saturation and conductivity modulation are also observed.

![Graph showing conductivity modulation and velocity saturation with avalanche]

![Diagram of NPN transistor with labeled regions]
Model Development

Using MEXTRAM to Model Collector-Emitter Breakdown:

- Weak avalanche is modelled in MEXTRAM.
- The resulting current will turn-on the Emitter-Base diode.
- This is sufficient to initiate and sustain the breakdown.
- The collector resistance will be optimized to model the conductivity modulation.
- Velocity saturation is also modelled in MEXTRAM.
Model Development

Collector-Emitter Breakdown Model

NPN

PNP

NPN $A_E=1\times10\mu m$

Device Failure $(V_M,I_M)$

$BV_{CEO}$

PNP $A_E=1\times10\mu m$

Device Failure $(V_M,I_M)$

$BV_{CEO}$
Model Development

Bipolar Model for ESD Event Simulations

CBO Model

EBO Model

MEXTRAM
Model Development

Failure Metric

- Difficult to Model
- Empirical formulation
  - Current density
  - Energy dissipation
Model Development

Failure Metric

- Difficult to Model
- Empirical formulation
  - Current density
  - Energy dissipation

![Graph showing Maximum Current (mA) vs. Emitter Area (μm²) for NPN and PNP types with a 100 ns pulse.](image-url)
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Circuit Simulation Example

Full-Chip ESD Simulation

- High frequency RF quadrature modulator
- Required to pass 2,000V HBM
- ESD simulation mimics actual HBM testing
Circuit Simulation Example

Full-Chip ESD Simulation

The design failed 1,000V HBM when stressed between supply $V_{CC}$ and the I/O pin ($V_{OUT}$).

![Diagram showing a failed NPN transistor](image)
The simulation identified NPN Q9 to go into $BV_{CEO}$ and conduct current before the ESD protection turns on.
Circuit Simulation Example

- Current and Voltage transient of NPN transistor Q9 during HBM stress with failure region highlighted.
Circuit Simulation Example

- XIVA (eXternally-Induced Voltage Alteration) micrograph
- The failure location identified was the output NPN transistor flagged by the ESD simulator.

Device Failure: Q9
Circuit Simulation Example

- Fix consists of adding resistor in series with transistor Q9
- Resulting current through transistor Q9 decreases to below failure level.
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SUMMARY

- An enhanced compact bipolar breakdown model was developed for a SiGe bipolar process.

- The model was built around the industry-standard MEXTRAM compact bipolar model, enabling SPICE-like circuit simulation.

- The model developed is integrated as part of the standard SPICE-type circuit simulation environment.

- Simulation accuracy was confirmed using circuit simulation example and the relevant Failure Analysis techniques.

- Predictive ESD simulation methodology used successfully on over four dozen designs, over four bipolar process technologies and on various design complexities.
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